REMARKS

The above-identified Divisional Application is being filed based on original claim 1. Prior to examination of the Divisional Application, Applicant is adding claims 6 and 7 for consideration when the application is examined.

In addition, Applicant is correcting a typographical error in line 23 of page 17 of the specification, where there is erroneous reference to "30-50 mm". As correctly set forth in line 6 of page 4, the reference should be to "30-50 nm". Line 23 of page 17 is being amended to correct this error. Marked up versions of the replacement paragraphs of the specification are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii).

Therefore, an action on the merits of claims 1, 6 and 7 is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: November 14, 2001

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Version with markings to show changes made:

IN THE SPECIFICATION:

Rewrite the paragraph which begins on line 22 of page 17 as follows:

(3) On the back surface, there remained grinding striations as micro roughness having a P-V value of about 30 to 50 [mm] nm and an interval of about 1 to 10 mm. However, they were very fine, and therefore, the grinding striations on the back surface were not transferred to the front surface of the wafer when the wafer was chucked during device process.

IN THE CLAIMS:

Please add the following new claims 6 and 7:

--6. (New) A semiconductor wafer, wherein the wafer has opposite front and back surfaces, the front surface is subjected to a finishing mirror-polishing without being subjected to surface-grinding, and micro roughness formed during surface grinding remains on the back surface. --

--7. (New) The semiconductor wafer according to claim 6, wherein the micro roughness on the back surface has P-V value of 30 to 50 nm and intervals of 1 to 10 mm. --